

Product Specification

8" COLOR TFT-LCD MODULE

Model Name: C080VAN02.3

< ◆ > Preliminary Specification

< > Final Specification

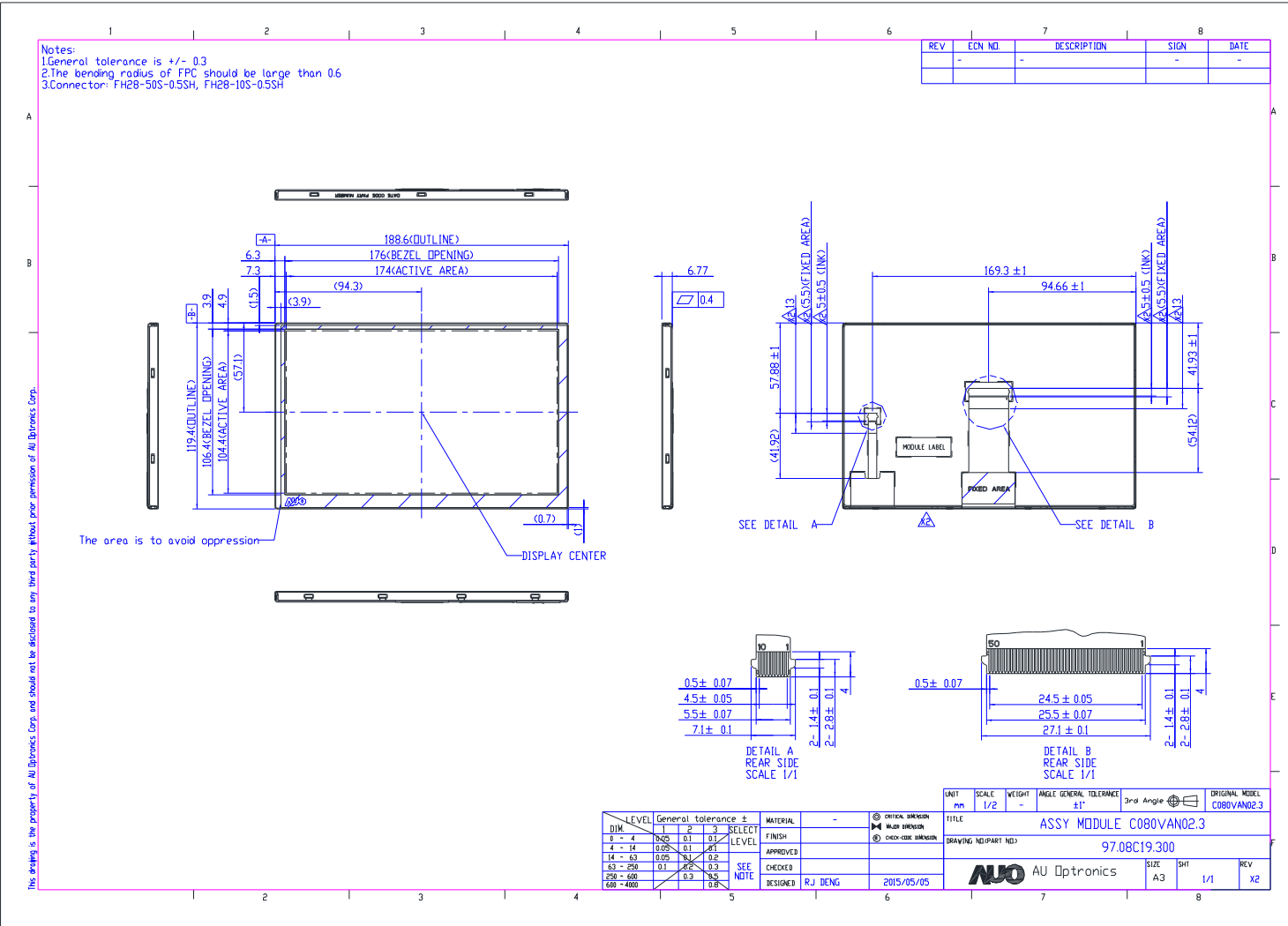
Note: The content of this specification is subject to change.

© 2015 AU Optronics
All Rights Reserved,
Do Not Copy.

A. Physical Specifications

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800 (H)×480 RGB(V)	
2	Active Area	mm	174(H)×104.4(V)	
3	Screen Size	inch	8(Diagonal)	
4	Dot Pitch	mm	0.2175(H)×0.0725×RGB(V)	
5	Color Configuration	--	R. G. B. Horizontal Stripe	Note 1
6	Color Depth	--	16.7M Colors	
7	Overall Dimension	mm	188.6 (H) x 119.4 (V) x 6.77 (T)	Note 2
8	Weight	g	208±10%	
9	Display Mode	--	Normally Black	
10	Surface Treatment		AG	

B. Outline Dimension



C. Electrical Specifications

1. Pin Assignment

a. Main FPC

Connector = HROSE,FH28-50S-0.5SH

No.	Pin Name	I/O	Description	Remarks
1	MODE	I	HV or DE selection	Note 1
2	UPDN	I	Vertical scan direction control. "H"→ Down to Up; "L"→ Up to Down	Note 2
3	SHLR	I	Horizontal scan direction control. "H"→ Left to Right; "L"→ Right to Left	Note 2
4	GND1	-	Ground	
5	DE	I	Data Input Enable	
6	VS	I	Vertical Sync	
7	HS	I	Horizontal Sync	
8	GND2	-	Ground	
9	DCLK	I	Clock For Input Data	
10	GND3	-	Ground	
11	DR7	I	Red Data7	
12	DR6	I	Red Data6	
13	DR5	I	Red Data5	
14	DR4	I	Red Data4	
15	DR3	I	Red Data3	
16	DR2	I	Red Data2	
17	DR1	I	Red Data1	
18	DR0	I	Red Data0	
19	DG7	I	Green Data7	
20	DG6	I	Green Data6	
21	DG5	I	Green Data5	
22	DG4	I	Green Data4	
23	DG3	I	Green Data3	
24	DG2	I	Green Data2	
25	DG1	I	Green Data1	
26	DG0	I	Green Data0	
27	DB7	I	Blue Data6	
28	DB6	I	Blue Data7	
29	DB5	I	Blue Data5	
30	DB4	I	Blue Data4	
31	DB3	I	Blue Data3	
32	DB2	I	Blue Data2	
33	DB1	I	Blue Data1	
34	DB0	I	Blue Data0	
35	GND4	-	Ground	
36	AVDD	P	Power for analog	
37	RSTB	I	Reset	

38	VDD1	P	Power for Logic	
39	VDD2	P	Power for Logic	
40	GND5	-	Ground	
41	CS	I	SPI signal	Note 3
42	SCL	I	SPI signal	Note 3
43	SDO	O	SPI signal	Note 3
44	SDA	I	SPI signal	Note 3
45	VCOM	P	Common electrode driving voltage	
46	GND6	-	Ground	
47	VGH	P	Positive power supply voltage for Gate driver	
48	GND7	-	Ground	
49	VGL	P	Negative power supply voltage for Gate driver	
50	GND8	-	Ground	

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Supply Voltage	VDD	-0.3	4.5	V	Note 1
Analog Input Voltage	AVDD	-0.5	15	V	Note 1
Gate Driver Voltage	VGH-VGL	-0.3	40	V	
	VGL	-20	0.3		
LED Power Consumption		3.2	4.3	W	
Storage Temperature	T _{ST}	-40	+95	°C	
Operating Temperature	T _{OP}	-30	+85	°C	

3. DC Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

a. Power Specification

Operating Voltage

Parameter	Symbol	Min	Typ.	Max.	Unit	Notes
Power Supply	VDD	3.0	3.3	3.6	V	
	AVDD	12.9	13	13.1	V	
	VGH	19.5	20	20.5	V	
	VGL	-8.5	-8	-7.5	V	
	VCOM		5.35		V	UPDN = L
			5.35		V	UPDN = H
Input high voltage	Vh	0.7*VDD	-	VDD	V	
Input low voltage	VI	GND	-	0.3*VDD	V	

b. Panel Loading

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Panel current	IVDD	-	16	20	mA	Note 1
	IAVDD	-	14	18	mA	
	IVGH	-	2	3.5	mA	
	IVGL	-	2	3.5	mA	
	Ivcom	-	2.5	5.5	mA	

4. AC Electrical Characteristics

a. Power on/off sequence

The LCD adopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:

Panel Power on sequence:

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	--	--	20	ms
T2	1	--	--	ms
T3	20	--	--	ms
T4	1	--	--	ms
T5	1	--	--	ms
T6	16.7	--	--	ms
T7	50	--	--	ms

Panel Power off sequence:

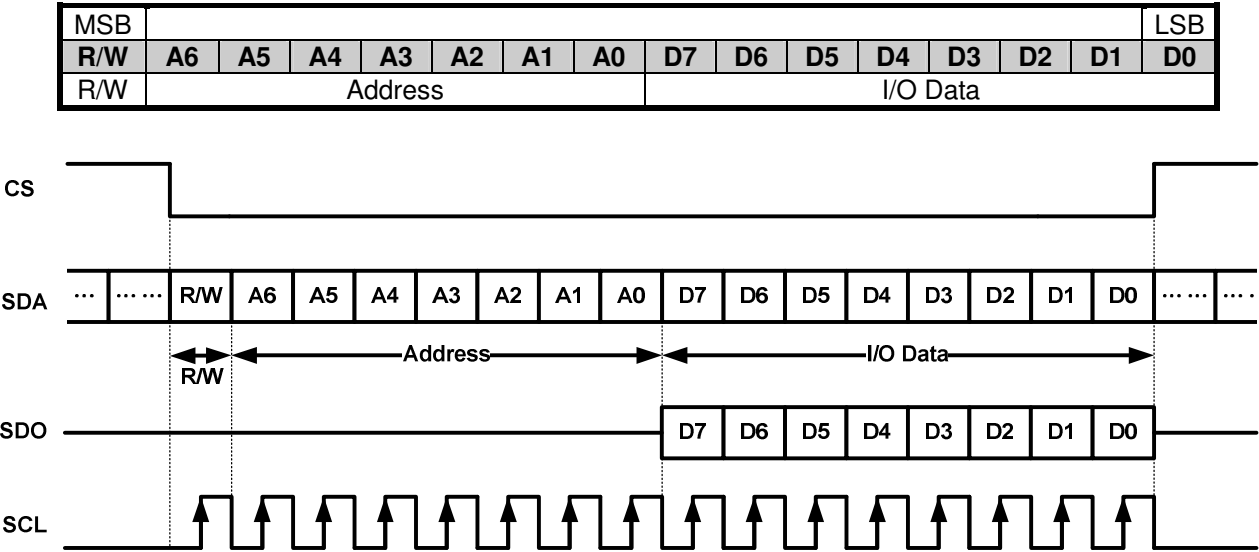
Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	0	--	-	ms
T2	20	--	-	ms
T3	6	--	-	ms
T4	40	--	--	ms
T5	0	--	--	us
T6	0	--	--	us

All signal must be discharge to zero voltage when power off.

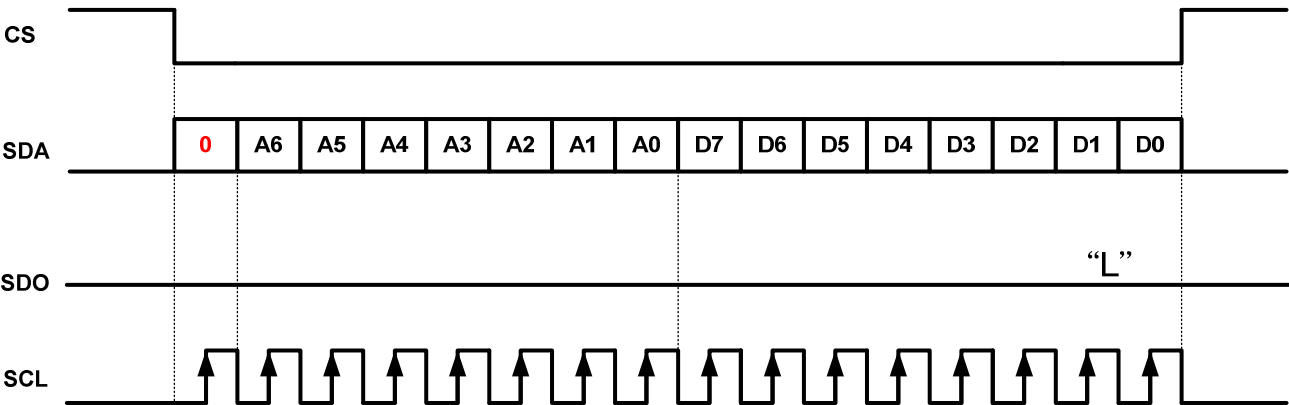
a. Timing Condition

Item	Symbol	Min	Typ	Max	Unit	Remark
Clock frequency	F_{CLK}	26.0	26.2	30	MHZ	
Vertical display area	T_{VD}	480				
Vertical period area	T_V	503	505	526	H	
Vertical blanking area	T_{VB}	23	25	46	H	Note1
Vertical pulse width	T_{VPW}	3				
Vertical back porch	T_{VBP}	20				
Vertical front porch	T_{VFP}	3	5	26	H	
Horizontal display area	T_{HD}	800				
Horizontal period area	T_H	860	864	950	dclk	
Horizontal blanking area	T_{HB}	60	64	150	dclk	Note2
Horizontal pulse width	T_{HPW}	3				
Horizontal back porch	T_{HBP}	48				
Horizontal front porch	T_{HFP}	12	16	102	dclk	
Data setup time	T_{DS}	10	-	-	ns	
Data hold time	T_{DH}	10	-	-	ns	

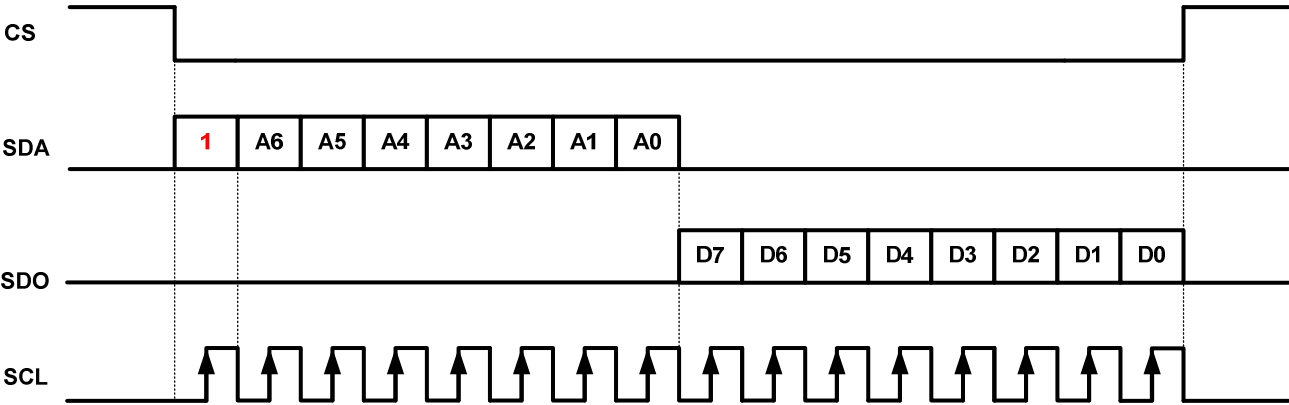
Timing chart



Write Mode:



Read Mode:



Register table

The setting flow can separate to 3 sections. First, determine V1, V9, V10 and V18. Second, choose V2, V8, V11 and V17. Third, choose V3, V7, V12 and V16. Last, choose V4, V5, V6, V13, V14 and V15.

Register address	Register data							
	D7	D6	D5	D4	D3	D2	D1	D0
R16H	1	1	VDDAG[5:0]					
R18H	0	0	0	0	Reg_VDDAG[3:0]			
R1EH	REGCTRL[7:0]							
R20H	1	0	0	V1(R) [4:0]				
R21H	0	0	0	V2(R) [4:0]				
R22H	0	0	0	V3(R) [4:0]				
R23H	0	0	0	V4(R) [4:0]				
R24H	0	0	0	V5(R) [4:0]				
R25H	0	0	0	V6(R) [4:0]				
R26H	0	0	0	V7(R) [4:0]				
R27H	0	0	0	V8(R) [4:0]				
R28H	0	0	0	V9(R) [4:0]				
R29H	0	0	0	V10(R) [4:0]				
R2AH	0	0	0	V11(R) [4:0]				
R2BH	0	0	0	V12(R) [4:0]				
R2CH	0	0	0	V13(R) [4:0]				
R2DH	0	0	0	V14(R) [4:0]				
R2EH	0	0	0	V15(R) [4:0]				
R2FH	0	0	0	V16(R) [4:0]				
R30H	0	0	0	V17(R) [4:0]				
R31H	0	0	0	V18(R) [4:0]				
R32H	0	0	0	V1(G) [4:0]				
R33H	0	0	0	V2(G) [4:0]				
R34H	0	0	0	V3(G) [4:0]				
R35H	0	0	0	V4(G) [4:0]				
R36H	0	0	0	V5(G) [4:0]				
R37H	0	0	0	V6(G) [4:0]				
R38H	0	0	0	V7(G) [4:0]				
R39H	0	0	0	V8(G) [4:0]				
R3AH	0	0	0	V9(G) [4:0]				
R3BH	0	0	0	V10(G) [4:0]				
R3CH	0	0	0	V11(G) [4:0]				
R3DH	0	0	0	V12(G) [4:0]				
R3EH	0	0	0	V13(G) [4:0]				
R3FH	0	0	0	V14(G) [4:0]				
R40H	0	0	0	V15(G) [4:0]				
R41H	0	0	0	V16(G) [4:0]				
R42H	0	0	0	V17(G) [4:0]				
R43H	0	0	0	V18(G) [4:0]				
R44H	0	0	0	V1(B) [4:0]				
R45H	0	0	0	V2(B) [4:0]				

R46H	0	0	0	V3(B) [4:0]
R47H	0	0	0	V4(B) [4:0]
R48H	0	0	0	V5(B) [4:0]
R49H	0	0	0	V6(B) [4:0]
R4AH	0	0	0	V7(B) [4:0]
R4BH	0	0	0	V8(B) [4:0]
R4CH	0	0	0	V9(B) [4:0]
R4DH	0	0	0	V10(B) [4:0]
R4EH	0	0	0	V11(B) [4:0]
R4FH	0	0	0	V12(B) [4:0]
R50H	0	0	0	V13(B) [4:0]
R51H	0	0	0	V14(B) [4:0]
R52H	0	0	0	V15(B) [4:0]
R53H	0	0	0	V16(B) [4:0]
R54H	0	0	0	V17(B) [4:0]
R55H	0	0	0	V18(B) [4:0]

R16h Control Register

Bit	Name	Function
Bit[5:0]	VDDAG	Voltage setting of VDDAG

R18h Control Register

Bit	Name	Function
Bit[3:0]	Reg_VDDAG	Enable VDDAG register. Set "1011" to enable VDDAG[5:0].

R1Eh Control Register

Bit	Name	Function
Bit[7:0]	REGCTRL	Register control enable. REGCTRL = AAh.(Default)

R20h Gamma Register

Bit	Name	Function
Bit[7]	Reg_Gam	Gamma register enable. Reg_Gam="0", disable gamma registers. (Default) Reg_Gam="1", enable gamma registers. Note: set Reg_Gam to "1" for adjusting gamma. Otherwise, gamma registers will keep the default value setting.
Bit[4:0]	V1(R)	$V1(R) = GMAH \times (169 + (V1R)_D) / 200$

R21h Gamma Register

Bit	Name	Function
Bit[4:0]	V2(R)	$V2(R) = V9(R) + (V1(R) - V9(R)) \times (69 + (V2R)_D) / 100$

R22h Gamma Register

Bit	Name	Function
Bit[4:0]	V3(R)	$V3(R) = V8(R) + (V2(R) - V8(R)) \times (59 + (V3R)_D) / 100$

R23h Gamma Register

Bit	Name	Function
Bit[4:0]	V4(R)	$V4(R) = V7(R) + (V3(R) - V7(R)) \times (55 + (V4R)_D) / 100$

R24h Gamma Register

Bit	Name	Function
Bit[4:0]	V5(R)	$V5(R) = V7(R) + (V3(R) - V7(R)) \times (26 + (V5R)_D) / 100$

R25h Gamma Register

Bit	Name	Function
Bit[4:0]	V6(R)	$V6(R) = V7(R) + (V3(R) - V7(R)) \times (3 + (V6R)_D) / 100$

R26h Gamma Register

Bit	Name	Function
Bit[4:0]	V7(R)	$V7(R) = V8(R) + (V2(R) - V8(R)) \times (8 + (V7R)_D) / 100$

R27h Gamma Register

Bit	Name	Function
Bit[4:0]	V8(R)	$V8(R) = V9(R) + (V1(R) - V9(R)) \times (V8R)_D / 100$

R28h Gamma Register

Bit	Name	Function
Bit[4:0]	V9(R)	$V9(R) = GMAH \times (95 + (V9R)_D) / 200$

R29h Gamma Register

Bit	Name	Function
Bit[4:0]	V10(R)	$V10(R) = GMAH \times (118 - (V10R)_D) / 200$

R2Ah Gamma Register

Bit	Name	Function
Bit[4:0]	V11(R)	$V11(R) = V10(R) - (V10(R) - V18(R)) \times (V11R)_D / 100$

R2Bh Gamma Register

Bit	Name	Function
Bit[4:0]	V12(R)	$V12(R) = V11(R) - (V11(R) - V17(R)) \times (8 + (V12R)_D) / 100$

R2Ch Gamma Register

Bit	Name	Function
Bit[4:0]	V13(R)	$V13(R) = V12(R) - (V12(R) - V16(R)) \times (V13R)_D / 100$

R2Dh Gamma Register

Bit	Name	Function
Bit[4:0]	V14(R)	$V14(R) = V12(R) - (V12(R) - V16(R)) \times (26 + (V14R)_D) / 100$

R2Eh Gamma Register

Bit	Name	Function
Bit[4:0]	V15(R)	$V15(R) = V12(R) - (V12(R) - V16(R)) \times (62 + (V15R)_D) / 100$

R2Fh Gamma Register

Bit	Name	Function
Bit[4:0]	V16(R)	$V16(R) = V11(R) - (V11(R) - V17(R)) \times (57 + (V16R)_D) / 100$

R30h Gamma Register

Bit	Name	Function
Bit[4:0]	V17(R)	$V17(R) = V10(R) - (V10(R) - V18(R)) \times (69 + (V17R)_D) / 100$

R31h Gamma Register

Bit	Name	Function
Bit[4:0]	V18(R)	$V18(R) = GMAH \times (31 - (V18R)_D) / 200$

Note 1. The tuning method of R, G and B are the same.

Note 2. Hardware control pin priority over register setting.

Note 3. GMAH = VDDAG

Register command flow (Tentative)

No.	Register address	Register data	
1	R1EH	10101010(AAH)	Note 1.
2	R18H	00001011(0BH)	
3	R16H	11101101(EDH)	
4	R20H	10010101(95H)	
5	R32H	00010101(15H)	
6	R44H	00010101(15H)	
7	R28H	00001011(0BH)	
8	R3AH	00001011(0BH)	
9	R4CH	00001011(0BH)	
10	R29H	00010110(16H)	
11	R3BH	00010110(16H)	
12	R4DH	00010110(16H)	
13	R31H	00001111(0FH)	
14	R43H	00001111(0FH)	
15	R55H	00001111(0FH)	
16	R21H	00011101(1DH)	
17	R33H	00011101(1DH)	
18	R45H	00011101(1DH)	
19	R27H	00000000(00H)	
20	R39H	00000000(00H)	
21	R4BH	00000000(00H)	
22	R2AH	00000000(00H)	
23	R3CH	00000000(00H)	
24	R4EH	00000000(00H)	
25	R30H	00011101(1DH)	
26	R42H	00011101(1DH)	
27	R54H	00011101(1DH)	
28	R22H	00010000(10H)	
29	R34H	00010000(10H)	
30	R46H	00010000(10H)	
31	R26H	00010011(13H)	
32	R38H	00010011(13H)	
33	R4AH	00010011(13H)	
34	R2BH	00010011(13H)	

35	R3DH	00010011(13H)	
36	R4FH	00010011(13H)	
37	R2FH	00010010(12H)	
38	R41H	00010010(12H)	
39	R53H	00010010(12H)	
40	R23H	00010100(14H)	
41	R35H	00010100(14H)	
42	R47H	00010100(14H)	
43	R24H	00010100(14H)	
44	R36H	00010100(14H)	
45	R48H	00010100(14H)	
46	R25H	00010010(12H)	
47	R37H	00010010(12H)	
48	R49H	00010010(12H)	
49	R2CH	00010110(16H)	
50	R3EH	00010110(16H)	
51	R50H	00010110(16H)	
52	R2DH	00010110(16H)	
53	R3FH	00010110(16H)	
54	R51H	00010110(16H)	
55	R2EH	00001110(0EH)	
56	R40H	00001110(0EH)	
57	R52H	00001110(0EH)	

Note 1. R1EH set to 8h'AA to enable register-control-only registers.

D. Optical specifications (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time	Tr+Tf	25℃	25	-	-	ms	Note 3
		-30℃	500				
Contrast ratio	CR	$\theta=0^\circ$	800	-	-		Note 4, 5, 6
Viewing Angle Top Bottom Left Right		$CR \geq 175$			20 10 50 50	deg.	Note 7, 8
Brightness	Y_L	$\theta=0^\circ$	650	820	-	cd/m ²	Note 1,2,9

E. Reliability Test Items (Note 2)

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 95℃	240Hrs	Note1
2	Low temperature storage	Ta= -40℃	240Hrs	
3	High temperature operation	Ta= 85℃	240Hrs	
4	Low temperature operation	Ta= -30℃	240Hrs	Note1, 3
5	High temperature and high humidity	Ta= 60℃, 90% RH	240Hrs	Operation
6	Heat shock	-30℃~85℃/100 cycles 1Hrs/cycle		Non-operation
7	Electrostatic discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B		Operation (Note 4)