



深圳市鑫航盛科技有限公司  
SHENZHEN XINHANGSHENG TECHNOLOGY CO., LTD

产品规格书

Product Type: 9.7" TFT LCD Module

LCD Nunmber: WD097GHL40AA-A8

MODULE NO. :

CUSTOMER APPROVED	PREPARE BY	CHECK BY	APPROVED BY
SUPPLIER APPROVED	PREPARE BY	CHECK BY	APPROVED BY

☒ Preliminary Specification

☐ Final Specific



## 1. OVERVIEW

### 1.1 Introduction

WD097GHL40AA-A is 9.7" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit and LED backlight. By applying 1024×768 images are displayed on the 9.7" diagonal screen. Display 16.7M colors by R.G.B signal input.

General specification are summarized in the following table:

### 1.2 Features

- 9.7 (4:3 diagonal) inch configuration
- 16.7M color by 6 bit input
- RoHS Compliance
- Halogen Free

Item	Specification	Unit
Screen Diagonal	9.7	Inch
Active area	196.608 x 147.456	mm
Pixels (HxV)	1024x3(RGB)X768	-
Pixel Pitch	0.192 (H) x 0.192 (V)	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally White	-
Contrast Ratio	(500) (Typ.)	-
Response Time	(20) (Typ.)	ms
Input Voltage	3.7V	V
Interface	LVDS	
Module size	210.20x164.20x4.85mm	mm
Support Color	262,144	
Weight	TBD	g
Surface treatment	Hard Coating	



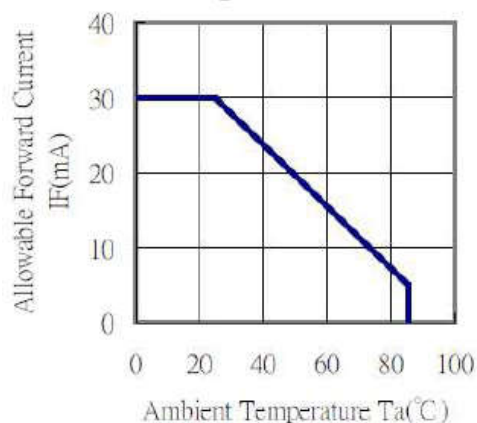
## 2. ABSOLUTE MAXIMUM RATINGS

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	DVDD DVDD_LVDS	-0.3	7	V	
Analog Supply Voltage	AVDD	-0.5	14.85	V	
Gate On Voltage	VGH	-0.3	42	V	
Gate Off Voltage	VGL	-20	0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	12	40	V	
Signal Input Voltage	NIND0 ~ NIND3 PIND0 ~ PIND3 NINC,PINC	-0.5	5	V	
Forward Current (per LED)	If	-	30	mA	
Reverse Voltage (per LED)	VR	-	5	V	
Pulse forward current (per LED)	I <sub>fp</sub>	-	100	mA	1、2、3
Operating temperature	Topa	-20	70	°C	4
Storage temperature	Tstg	-30	80	°C	4

Note:

- \*1) If the product were used out of the operation and storage range, it will have quality issue.
- \*2) I<sub>fp</sub> Conditions : Pulse Width  $\leq$  10msec, Duty  $\leq$  1/10.
- \*3) Each one of LED operation must be follow diagram of Ambient Temperature and Allowable Forward Current.



- \*4) If users use the product out off the environmental operation range (temperature and humidity) , it will have visual quality concerns.



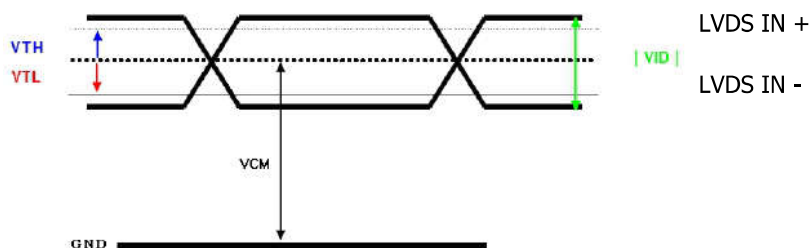
### 3. ELECTRICAL CHARACTERISTICS

#### 3.1 TFT LCD

Ta=25°C

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	DVDD	2.3	3.3	3.6	V	
Logic Input Voltage (LVDS:IN+,IN-)	VCM	$\frac{VID}{2}$	-	$2.4 \downarrow \frac{VID}{2}$	V	Note1
	VID	200	-	600	mV	Note1
	VTH	-	-	100	mV	VCM=1.2V Note1
	VTL	-100	-	-	mV	
Analog Power Supply Voltage	AVDD	9.35	9.6	TBD	V	
Gate On Power Supply Voltage	VGH	17	19	20	V	
Gate Off Power Supply Voltage	VGL	-10.6	-10	-9.5	V	
Common Power Supply Voltage	VCOM	3.5	(3.75)		V	Note2
Logic Input Voltage	VIH	0.7*DVDD	-	DVDD	V	
	VIL	GND	-	0.3*DVDD	V	

【Note1】 LVDS signal



【Note2】 Please adjust VCOM to make the flicker level be minimum.



### 3.2 TFT-LCD Current Consumption

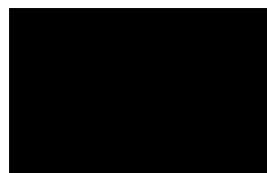
The following parameters are for reference only, With the actual debugging parameters as the standard

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note.
Gate on Current	IVGH	VGH = 19V	-	0.5	1	mA	【Note1】
Gate off Current	IVGL	VGL = -10V	-	0.5	1	mA	【Note1】
Digital Current	IDVDD	DVDD = 3.7V	-	25	35	mA	【Note1】
Analog Current	IAVDD	AVDD = 9.6V	-	25	35	mA	【Note1】
Total Power Consumption	PC		-	336	478.5	mW	【Note1】

【Note1】 Typical: Under 256 gray pattern  
Maximum: Under Black pattern



256 gray pattern

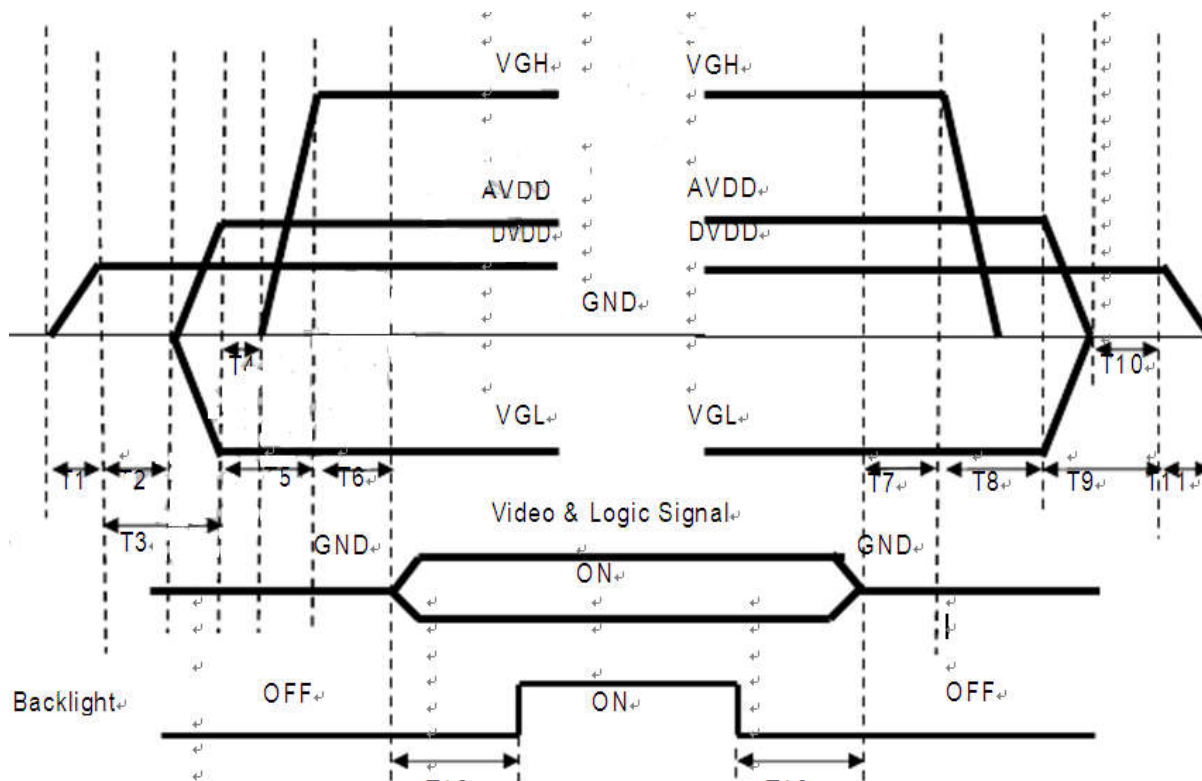


Black Pattern

### 3.3 Power and Signal sequence

Power On: DVDD→AVDD/VGL→VGH→Video & Logic Signal→Backlight

Power Off: Backlight→Video & Logic Signal→VGH→AVDD/VGL→DVDD



$0 < T1 \leq 10\text{ms}$   $T2 > 0\text{ms}$   $T3 > 20\text{ms}$   $T4 > 0\text{ms}$   $T5 > 10\text{ms}$   $0 < T6 \leq 10\text{ms}$   $T7 > 0\text{ms}$   
 $T8 > 0\text{ms}$   $T9 > 0\text{ms}$   $T10 > 0\text{ms}$   $0 < T6 \leq 10\text{ms}$   $0 < T11 \leq 10\text{ms}$   $T12 \geq 200\text{ms}$   $T13 \geq 200\text{ms}$



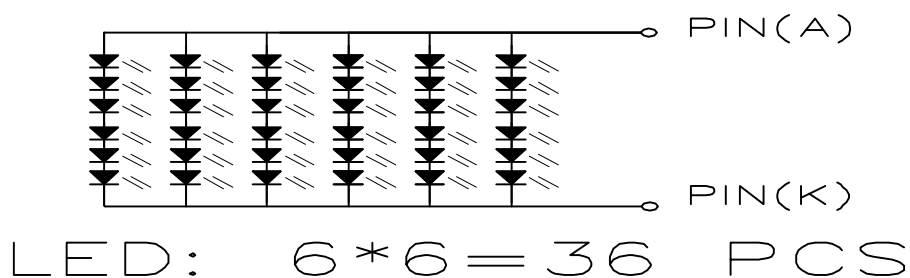
### 3.4 Backlight

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
LED current	IL	Ta=25℃ (20mA/serise)	--	150	--	mA	
LED voltage	VL	Ta=25℃ (20mA/serise)	16	18	19.8	V	
Power consumption	WL	Ta=25℃ (20mA/serise)	--	2.88	--	W	
LED Lifetime	-	Ta=25℃ IF=20mA	30000			Hr	

Remarks:

\*1)LED Circuit Diagram

## 线路原理图



\*2) A: Anode(+), K: Cathode(-)

\*3) Suggestion: Using the constant current control to avoid the leakage light and brightness quality issue.

\*4) Definition of Led lifetime: Luminance < Initial luminance 50%.



## 4. INTERFACE CONNECTION

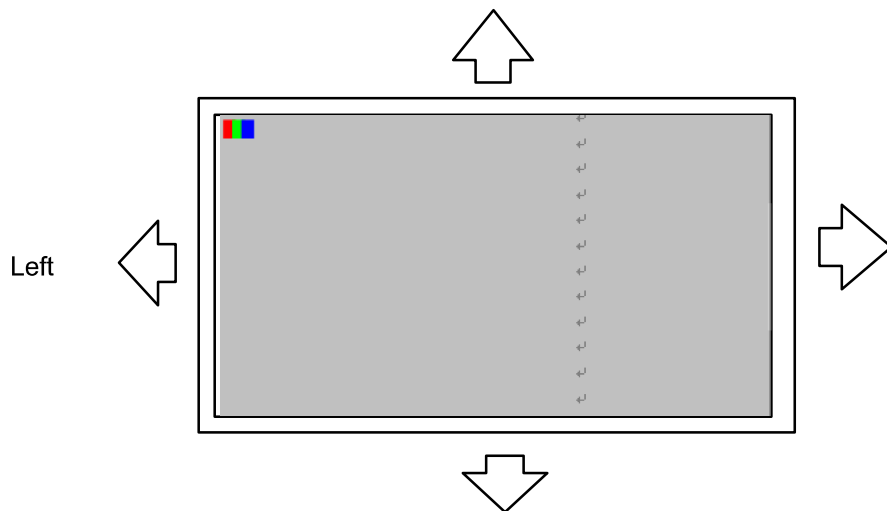
### 4.1 CN1 (Input Signal)

Pin No.	SYMBOL	FUNCTION	Note
1	VCOM	Common voltage	
2	DVDD	Digital power	
3	DVDD	Digital power	
4	NC	Not connect	
5	RESET	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10K , C=1μF)	
6	UPDN	Vertical inversion	Note 1
7	SHLR	Horizontal inversion	Note 1
8	STBYB	Standby mode, normally pull high STBYB="1", normal operation STBYB="0", timing control, source driver will turn off, all output are high-Z	
9	GND	Ground	
10	NINC	Negative LVDS differential clock input	
11	PINC	Positive LVDS differential clock input	
12	GND	Ground	
13	NIND0	Negative LVDS differential data input	
14	PIND0	Positive LVDS differential data input	
15	GND	Ground	
16	NIND1	Negative LVDS differential data input	
17	PIND1	Positive LVDS differential data input	
18	GND	Ground	
19	NIND2	Negative LVDS differential data input	
20	PIND2	Positive LVDS differential data input	
21	GND	Ground	
22	NIND3	Negative LVDS differential data input	
23	PIND3	Positive LVDS differential data input	
24	GND	Ground	
25	SELB	6bit/8bit mode select if LVDS input data is 6bits, SELB set to High if LVDS input data is 8bits, SELB set to Low	
26	GND	Ground	
27	AVDD	Power for Analog Circuit	
28	GND	Ground	
29	VGH	Positive power for TFT	
30	NC	Not connect	
31	NC	Not connect	
32	VGL	Negative power for TFT	
33	GND	Ground	
34	NC	Not connect	
35	NC	Not connect	
36	NC	Not connect	
37	NC	Not connect	
38	NC	Not connect	
39	NC	Not connect	
40	NC	Not connect	



【Note1】UPDN and SHLR control function

SHLR	UPDN	Data shifting
DVDD	GND	Left→Right, Up→Down(default)
GND	GND	Right→Left, Up→Down
DVDD	DVDD	Left→Right, Down→Up
GND	DVDD	Right→Left, Down→Up







## 5.0 LVDS mode DC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Differential input high Threshold voltage	$R_{XVTH}$	-	-	+0.1	V	$R_{XVCM}=1.2V$
Differential input low threshold voltage	$R_{XVTL}$	-0.1	-	-	V	
Input voltage range (singled-end)	$R_{XVIN}$	0	-	$VDD-1.2+ V_{ID} /2$	V	-
Differential input common Mode voltage	$R_{XVCM}$	$ V_{ID} /2$	-	$VDD-1.2$	V	-
Differential input voltage	$ V_{ID} $	0.2	-	0.6	V	-
Differential input leakage Current	$R_{V_{XIIz}}$	-10	-	+10	$\mu A$	-
LVDS Digital Operating Current	$I_{ddlvds}$	-	15	30	mA	Fclk=65MHz, VDD=3.3V
LVDS Digital Stand-by Current	$I_{stlvds}$	-	10	50	$\mu A$	Clock & all Functions are stopped

Table 5.3: LVDS mode DC electrical characteristics

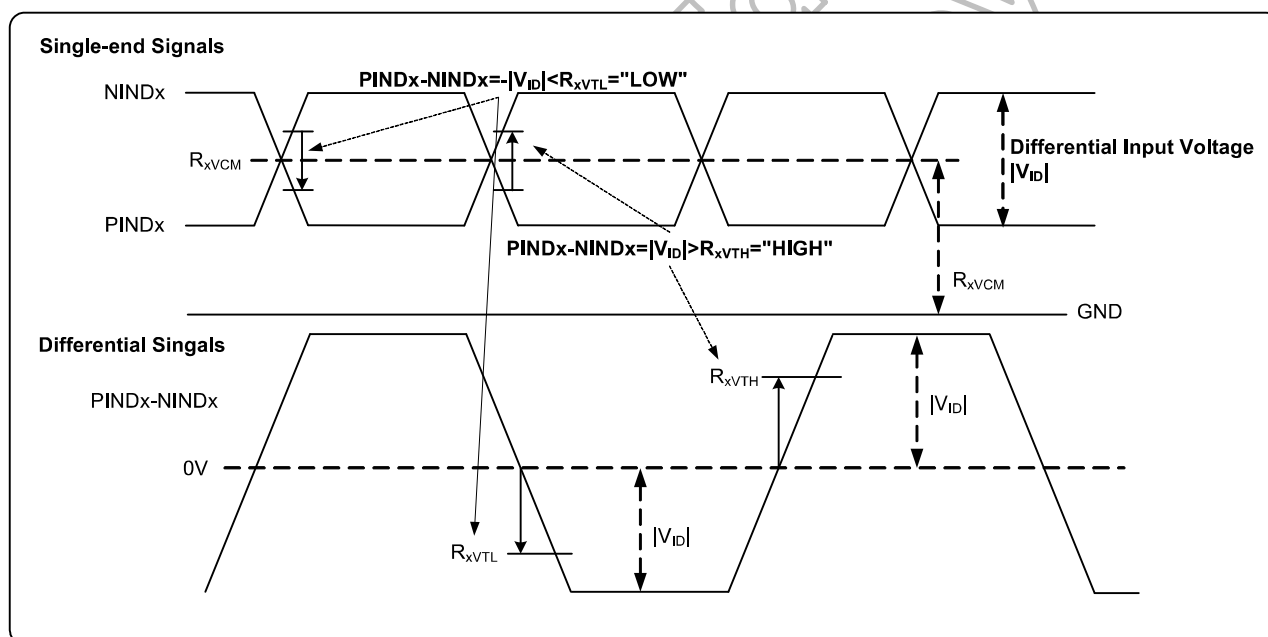


Figure 5.1: Single-end signals



The diagram illustrates the timing of a program segment on a 68000 microprocessor. It shows three signals: PINC, NINC, and three data bus signals (IND0, IND1, IND2) over 9 clock cycles. The signals are represented by horizontal lines for control and hexagonal blocks for data. The data bus signals are labeled with memory addresses: R0, G0, R5, R4, R3, R2, R1, R0, G0 for IND0; G1, B1, B0, G5, G4, G3, G2, G1, B1 for IND1; and B2, DE, VS, HS, B5, B4, B3, B2, DE for IND2. The signals are active during specific clock cycles, indicating the timing of data transfers.

Signal	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7	Cycle 8	Cycle 9
PINC	High	High	High	Low	Low	Low	High	High	High
NINC	High	High	High	Low	Low	Low	High	High	High
IND0	R0	G0	R5	R4	R3	R2	R1	R0	G0
IND1	G1	B1	B0	G5	G4	G3	G2	G1	B1
IND2	B2	DE	VS	HS	B5	B4	B3	B2	DE

Timing diagram for the 74VHC163 4-bit binary counter. The diagram shows the clock input (PINC) and the four data outputs (IND0, IND1, IND2, IND3) over time. The clock input is a square wave. The data outputs are shown as a sequence of hexagonal cells, each containing a value. The values for IND0 are R0, G0, R5, R4, R3, R2, R1, R0, G0. The values for IND1 are G1, B1, B0, G5, G4, G3, G2, G1, B1. The values for IND2 are B2, DE, VS, HS, B5, B4, B3, B2, DE. The values for IND3 are R6, -, B7, B6, G7, G6, R7, R6, -.

The diagram illustrates the timing requirements for the 74VHC163 4-bit binary counter. It shows the relationship between the clock input (CLKIN), data input (Data), data enable (DEN), clock output (CLKN), valid output signal (VSD), and high-impedance output signal (HSD). The timing parameters are defined as follows:

- CLKIN**: Clock input signal.
- Data**: Data input signal.
- DEN**: Data enable input signal.
- CLKN**: Clock output signal.
- VSD**: Valid output signal.
- HSD**: High-impedance output signal.

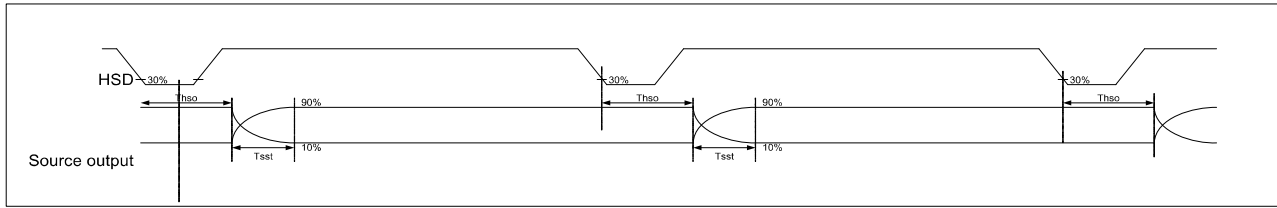
The timing parameters are defined as follows:

- Tcwl**: Clock-to-output delay (low-to-high).
- Tcph**: Clock-to-output delay (high-to-low).
- Tcwh**: Clock-to-output delay (high-to-low).
- Tdsu**: Data setup time.
- Tdhd**: Data hold time.
- Tdsu**: Data setup time.
- Tdhd**: Data hold time.
- Tst**: Setup time.
- Thhd**: Hold time (high-to-low).
- Thst**: Hold time (low-to-high).
- Th**: Hold time.

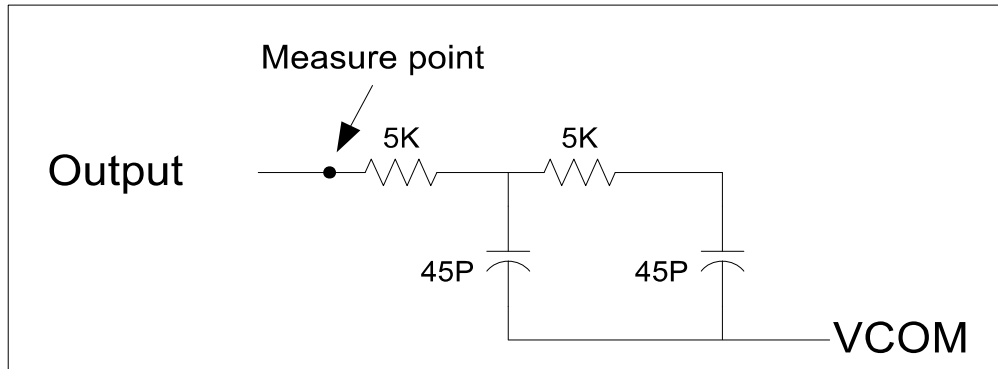
### Input clock and data timing diagram



#### 5.2.4 Source output timing diagram (Cascade)



Source output timing diagram



- DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	52	65	71	MHz
Horizontal Display Area	thd	1024			DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd	768			T <sub>H</sub>
VSD Period	tv	778	806	845	T <sub>H</sub>
VSD Blanking	tvbp+ tvfp	10	38	77	T <sub>H</sub>

DE mode (1024x768)

- HV mode

#### Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	57	65	70.5	MHz
Horizontal Display Area	thd	1024			DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp	160			DCLK
HSD Front Porch	thfp	16	160	216	DCLK

HV mode horizontal timing (1024x768)

#### Vertical timing

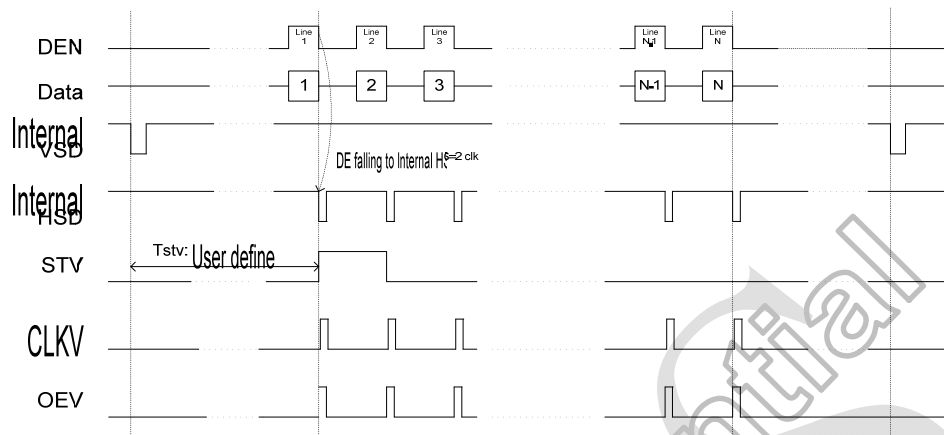
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd	768			T <sub>H</sub>
VSD Period	tv	792	806	840	T <sub>H</sub>
VSD Pulse Width	tvpw	1	-	20	T <sub>H</sub>
VSD Back Porch	tvbp	23			T <sub>H</sub>
VSD Front Porch	tvfp	1	15	49	T <sub>H</sub>

HV mode vertical timing (1024x768)



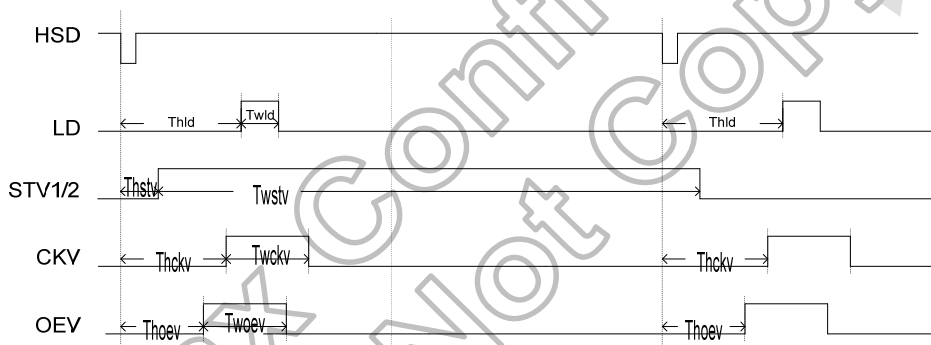
## 5.3 Output Timing

### 5.3.1 Vertical timing diagram DE (Cascade)



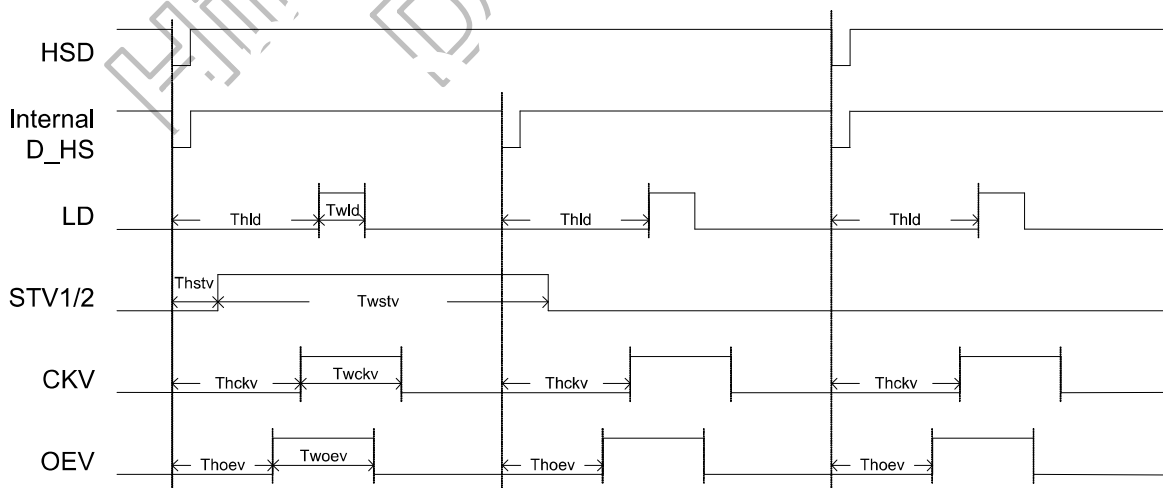
Vertical timing diagram DE (Cascade)

### 5.3.2 Gate output timing diagram (Cascade)



Gate output timing diagram (Cascade)

### 5.3.3 Gate output timing diagram (Dual gate)



Gate output timing diagram (Dual gate)



## 5.4 Color Data Reference

[illegible]

Note :

- 1) Gray level:  
Color(n): n is level order; higher n means brighter level.
- 2) DATA:  
1: high, 0: low





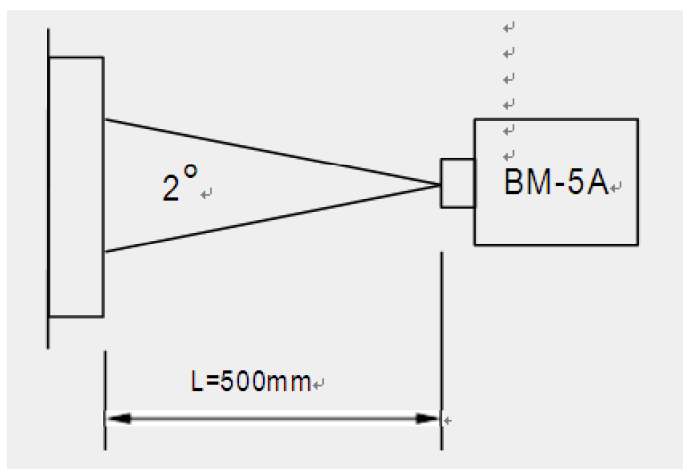


## 7. OPTICAL CHARACTERISTICS

Ta = 25°C, Vcc=3.3V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Luminance(CEN)		Lw		400	420	—	cd/m <sup>2</sup>	
Contrast		CR	Θ=0 Normal viewing angle	400	500	—		(1)(2)
Response time		Tr		—	6	12	msec	(1)(3)
		Tf		—	14	20		
Color gamut		S		45	50	—	%	C light
Color chromaticity (CIE1931)	Red	R <sub>x</sub>		-0.02	0.620	+0.02		(1)(4) CF Glass C light
		R <sub>Y</sub>			0.332			
	Green	G <sub>x</sub>			0.281			
		G <sub>Y</sub>			0.534			
	Blue	B <sub>x</sub>	0.146					
		B <sub>Y</sub>	0.131					
	White	W <sub>x</sub>	0.301					
		W <sub>y</sub>	0.326					
Viewing angle (With EWV PZ)	Hor.	Θ <sub>L</sub>	CR>10	80	85	—	(1)(4)	
		Θ <sub>R</sub>		65	75	—		
	Ver.	Θ <sub>U</sub>		75	85	—		
		Θ <sub>D</sub>		75	85	—		
Optima View Direction		9 o'clock						(5)

【Note1】 Measure condition: 25°C±2°C, 60±10%RH, under 10 Lux in the dark room. BM-5A (TOPCON), viewing angle 2°, IL=260mA (Backlight current), measurement after lighting on 10 mins.



【Note2】 Definition of contrast ratio:

Contrast Ratio (CR)= (White) Luminance of ON + (Black) Luminance of OFF



- 【Note3】 Definition of luminance: Measure white luminance on the point 5 as figure.7-1  
 Definition of Luminance Uniformity: Measure white luminance on the point1~9 as figure.7-1  

$$\Delta L = [L(\text{MIN})/L(\text{MAX})] \times 100$$

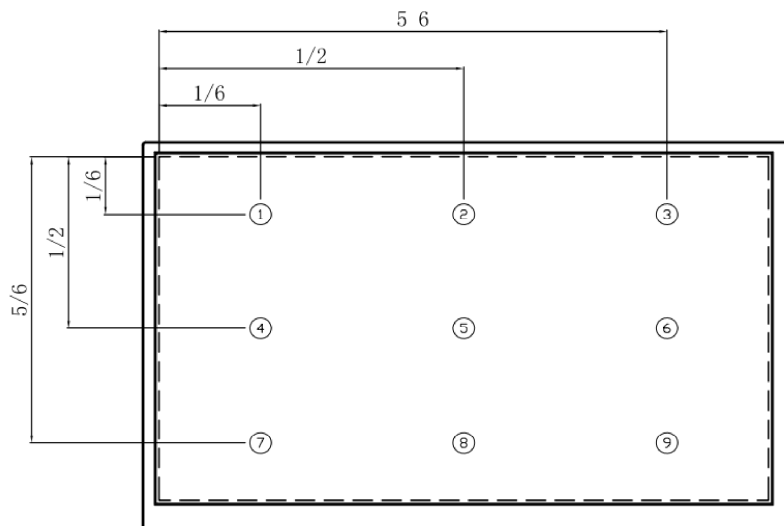
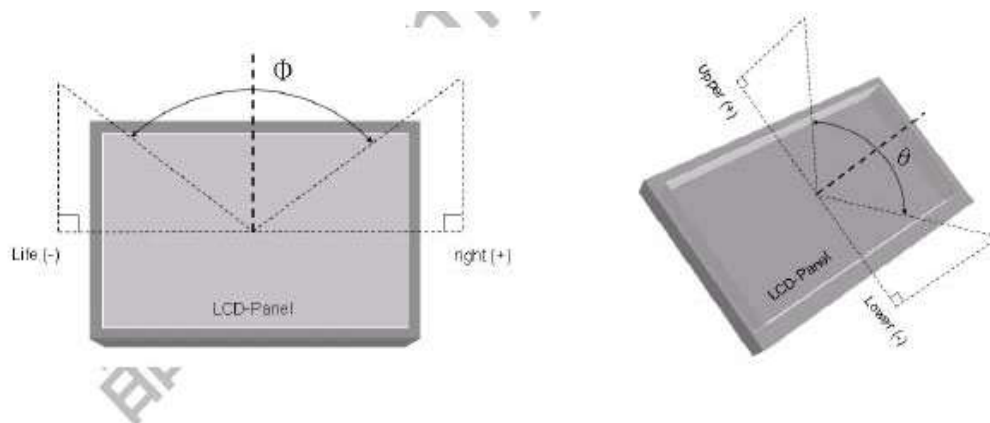
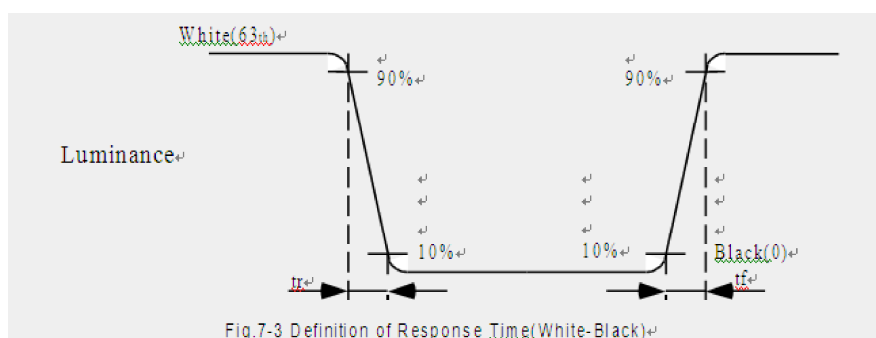


Fig.7-1 Measuring point

- 【Note4】 Definition of Viewing Angle( $\theta, \psi$ ), refer to Fig.7-2 as below:



- 【Note5】 Definition of Response Time.(White-Black)







## 8. RELIABILITY TEST

### 8.1. Temperature and humidity

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta= +80°C, 240hrs	
2	Low Temperature Storage	Ta= -30°C, 240hrs	
3	High Temperature Operation	Ta= +70°C, 240hrs	
4	Low Temperature Operation	Ta= -20°C, 240hrs	
5	Thermal Cycling Test (non operation)	-30°C(30min)→+70°	

【Note1】:

Condition of Image Sticking test: 25 °C± 2 °C

Operation with test pattern sustained for 4 hrs, then change to gray pattern immediately.

After 5 mins, the mura must be disappeared completely .

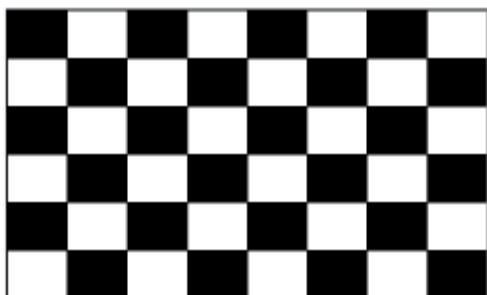


Image Sticking pattern



Mid-Gray pattern

### 8.2. Shock and Vibration

TEST ITEMS	CONDITIONS
Shock (Non-operation)	Shock level: 980m/s <sup>2</sup> (equal to 100G). Waveform: half sinusoidal wave, 6ms. Number of shocks: +X, +Y, +Z axes for a total of nine shock inputs.
Vibration (Non-operation)	Frequency range: 8~33.3Hz Stroke: 1.3 mm Vibration: sinusoidal wave, perpendicular axis (both x, z axis: 2hrs, y axis: 4hrs). Sweep: 2.9G, 33.3 Hz -400 Hz Cycle time: 15 min

### 8.3 Electrostatic Discharge

TEST ITEM	CONDITIONS	Note
ESD	150pF, 330 , ±8kV&±15kV air& contact test	1
	200pF, 0 , ±200V contact test	2

【Note】 Measure

1: LCD glass and metal bezel

2: IF connector pins

---

**Model** : 所有车载工控系列产品

标准：按原厂大板玻璃IIS执行除带点率控制在10%&A区无大于0.3的亮点）。

Customer Approved:	
Signature	Date
Supplier Approved:	
Signature	Date

# 深圳市鑫航盛科技有限公司

## SHENZHEN XINHANGSHENG TECHNOLOGY CO., LTD

### 1.0 Purpose:

Define the inspection criteria for Sheet total yield counting.

The total yield counting is 90% / Monthly base

### 2.0 Inspection condition is as following [Visual Inspection]

- Viewing distance is approximately 30 cm
- Viewing angle is normal to the LCD panel
- Ambient temperature:  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$
- Ambient illumination:  $1000 \pm 200$  Lux for Sheet appearance inspection
- Ambient illumination:  $100 \pm 50$  Lux for shorting bar test.
- B/L brightness is  $2000 \pm 200 \text{cd/m}^2$

### 3.0 Inspection criteria (Inspection criteria for sheet)

(HannStar will make a mark on the defect chip especially)

Item	Symptom	Judgment criteria
1/4 sheet appearance inspection  D: Diameter (Note 1)	Crack	Not allowed
	Chipping	No damage any pad and circuit
	Surface Stains / Dirt	1. The defect can be wiped by alcohol is acceptable. 2. Others are followed as: (Per chip) $D \leq 0.1\text{mm}$ , Ignore $0.1\text{mm} < D \leq 0.2\text{mm}$ , $N \leq 1$ $D > 0.2\text{mm}$ : Not Allowed
	Panel scratch of active area	1. Dummy area: don't care. 2. As L: don't care, $W \leq 0.05\text{mm} \rightarrow$ Ignore As $L \leq 3.0\text{mm}$ , $0.05\text{mm} < W \leq 0.08\text{mm} \rightarrow n \leq 4$ As $W > 0.08\text{mm}$ Not allowable
	Pad open or short circuit	Not allowed

D: diameter , N: number , W: horizontal width , L: vertical height

# 深圳市鑫航盛科技有限公司

SHENZHEN XINHANGSHENG TECHNOLOGY CO., LTD

## 4.0 Inspection criteria for light on test

### 4.1 Test pattern:

Test pattern	Description
Black	The driving waveform is defined in product spec. All visible defects are judged as the following inspection criteria, 4-2
Gray	
Red	
Green	
Blue	

### 4.2 Inspection criteria:

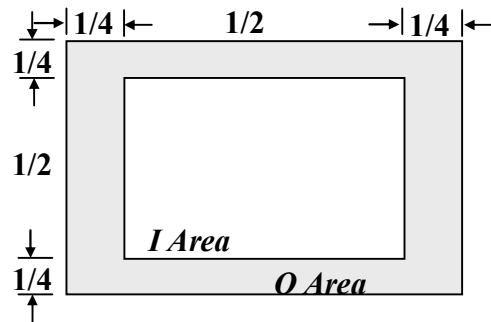
Item	Symptom	Judgment criteria		Note
Electrical defect	Area	I	O	Note 1.
	Bright dot	0	1	Note 2
	Dark dot	4	4	Note 2
	Distance between Bright - Bright	-		Note 3
	Distance between Dark- dark	$\geq 5\text{mm}$		Note 3.
	Distance between Bright - Dark	-		Note 3.
	Total Bright and Dark Dots	4		
	Line defect	Not Allowed		
	No Function	Not Allowed		
Visual defect	Black or white spot / particle	1. $D \leq 0.15\text{mm}$ : No count 2. $0.15\text{mm} < D \leq 0.4\text{mm}$ , $N \leq 3$ 3. $D > 0.4\text{mm}$ : Not allowable		Note 4
	Black or white line / particle (line)	0.05mm < W $\leq$ 0.1mm, 0.3mm < L $\leq$ 0.7mm, N $\leq$ 3 W > 0.1mm, L > 0.7mm: Not allowable		
	Mura	ND 5%		

D: diameter , N: number , W: horizontal width , L: vertical height

# 深圳市鑫航盛科技有限公司

## SHENZHEN XINHANGSHENG TECHNOLOGY CO., LTD

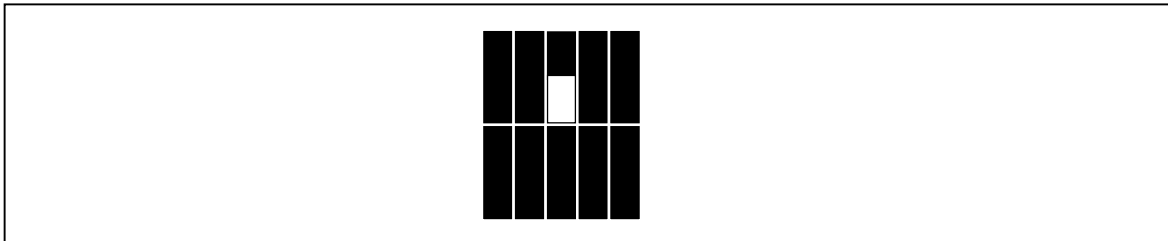
### Note 1 Definition of Area



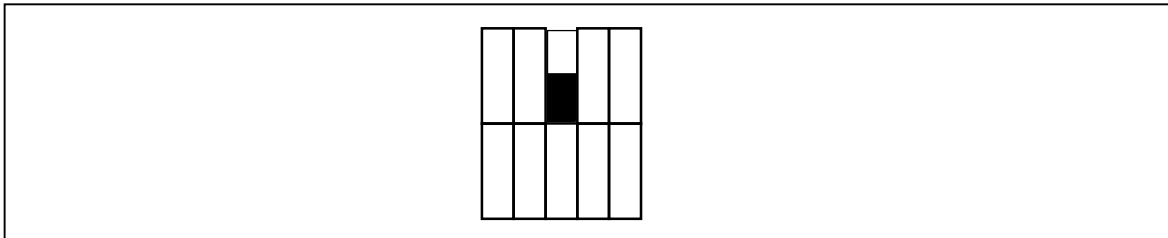
### Note 2. Bright, Dark dot defect description

-bright area is more than 50% of one dot

-Visible under : ND5%

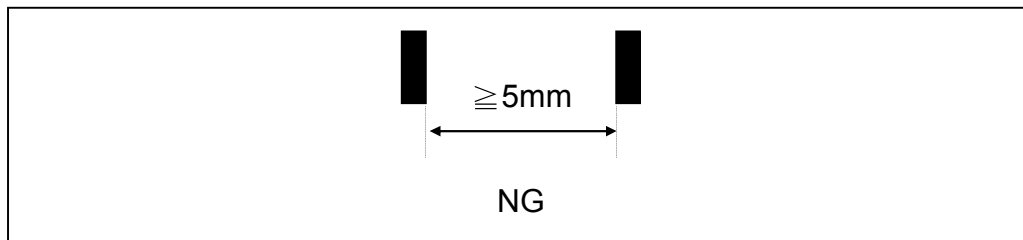


- dark area is more than 50% of one dot

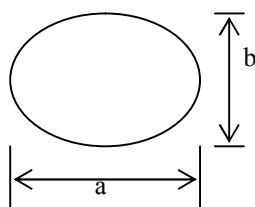


### Note 3. Minimum distance between dot defects

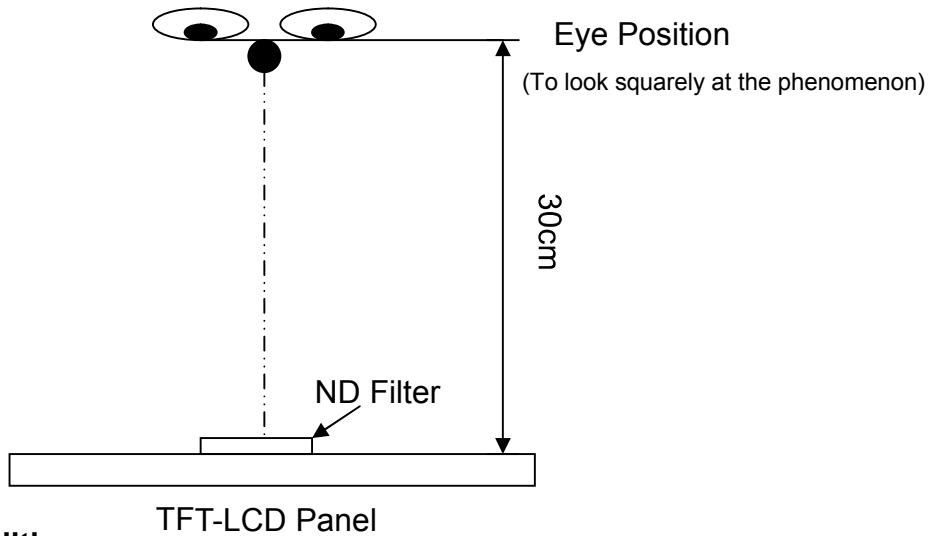
-Dark dot to Dark dot



### Note4. D : Diameter $D=(a+b)/2$



Note 5. Bright dot, mura and leak are defined through transmission ND Filter as following.



#### 5.0 Storage Condition

Storage temperature range :  $25\pm 5^{\circ}\text{C}$

Storage humidity range :  $50\pm 20\%\text{RH}$

#### 6.0 Life Time

Due to the product is Sheet shipping, to prevent quality problem caused by external environment, this product should be stored under storage condition as item 5.0 and finish LCD process within one month from receiving products.